WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device having a low dielectric interlayer insulation layer, the method comprising:

forming a silicon oxycarbide layer at a substrate;

treating the silicon oxycarbide layer with plasma; and

stacking a photoresist on the plasma-treated oxycarbide layer and patterning the resultant structure.

2. The method of Claim 1, wherein the silicon oxycarbide layer is formed by a CVD method by supplying a gas containing nitrogen atoms.

3. The method of Claim 2, wherein treating the silicon oxycarbide layer with plasma is performed by supplying at least one gas selected from the group consisting of He, H_2, N_2O, O_2 and Ar in a processing chamber where the substrate is installed.

4. The method of Claim 1, wherein forming the silicon oxycarbide layer and treating with plasma are performed in situ in a processing chamber for PECVD.

5. The method of Claim 4, wherein forming the silicon oxycarbide layer and treating with plasma are performed under conditions of a pressure of

1 to 10 Torr and a temperature of 300 to 400°C.

6. The method of Claim 1, wherein forming the silicon oxycarbide layer and treating with plasma are performed under conditions of a pressure of 1 to 10 Torr and a temperature of 300 to 400°C.

7. The method of Claim 1, wherein forming the silicon oxycarbide layer is performed using a gas of a methyl silane group as a source gas of carbon and silicon and using at least one of N_2O and O_2 for another source gas of oxygen, the methyl silane group that one or more hydrogen group of silane is substituted as a methyl group.

8. The method of Claim 1, wherein the photoresist is a chemical amplification type photoresist which generates hydrogen ions (H^+) in a case of light exposure.

9. The method of Claim 8, wherein the patterning comprises:

exposing the photoresist to light below a photo mask;

performing a post exposure bake; and

developing the photoresist.

10. The method of Claim 1, wherein the patterning comprises:

exposing the photoresist to light below a photo mask;

performing a post exposure bake; and

developing the photoresist.

11. A method of fabricating a semiconductor device having a low dielectric interlayer insulation layer, comprising:

stacking a silicon oxycarbide layer (SiOC) at a substrate;

treating the silicon oxycarbide layer with plasma; and

forming an interconnection at the silicon oxycarbide layer using a damascene process.

12. The method of Claim 11, wherein H_2-plasma is used for treating with plasma, and further comprising forming an insulation layer for capping on the silicon oxycarbide layer after treating with plasma and before forming the interconnection.

13. The method of Claim 12, wherein the insulation layer is formed of a PECVD layer by supplying at least one of a silane gas and a tetraethylorthosilicate (TEOS) gas.

14. The method of Claim 12, wherein treating with H_2-plasma is performed under a H_2-ambient at a temperature of 250 to 400°C and a pressure of 1 to 10 Torr and by applying a radio frequency electric field.

15. The method of Claim 12, wherein forming the interconnection using the damascene process comprises:

forming a photoresist pattern over the silicon oxycarbide layer;

forming a groove at the top of the silicon oxycarbide layer using the photoresist pattern as an etch mask;

removing the photoresist pattern by an ashing method using O_2-plasma at the groove-formed substrate;

sequentially stacking a barrier metal and a metal layer for interconnection at the groove-formed substrate to fill the groove; and

removing the metal layer for interconnection stacked at the top surface of the silicon oxycarbide layer using a chemical mechanical polishing (CMP) process.

16. The method of Claim 15, wherein the metal layer for interconnection is formed of copper.

17. The method of Claim 12, wherein the damascene process comprises forming the groove and then forming a contact hole at a region of the groove.

18. The method of Claim 12, wherein the silicon oxycarbide layer is formed by a spin on glass (SOG) technique.

19. The method of Claim 11, further comprising forming an organic polymer layer at the silicon oxycarbide layer using a coating method after treating with plasma and before forming the interconnection.

20. The method of claim 19, wherein stacking the silicon oxycarbide layer at the substrate is performed by at least one of an SOG coating method and a PECVD method.

21. The method of Claim 19, wherein forming the organic polymer layer is performed by a coating method at the substrate and then curing is performed at a high temperature of 400 to 450°C.

22. The method of Claim 19, wherein the damascene process is performed by a dual damascene method comprising forming a groove at the organic polymer layer using a patterning process and forming a contact hole at the silicon oxycarbide layer at a region of the groove through a patterning process.